

SYAZWAN S. D. ZULKEPLI

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PROFILE

MEng Electrical & Electronic Engineering graduate (2:1, University of Southampton) with hands-on experience in RF/antenna design (ANSYS HFSS), analogue circuit design, FPGA/digital design (SystemVerilog), and PCB design from schematic to bench. Seeking a graduate role in electronic hardware design, test or validation.

TECHNICAL SKILLS

- **RF, analogue & PCB:** Antenna design and simulation (ANSYS HFSS), analogue circuit design (op-amps, instrumentation and charge amplifiers), impedance matching, KiCad schematic capture and PCB layout, flexible PCB fabrication.
- **Digital & embedded:** SystemVerilog/Verilog RTL design, FPGA implementation and verification (Intel Quartus, Questa, Cyclone V), embedded C/C++, I2C/SPI/UART protocols.
- **Simulation & instrumentation:** ANSYS HFSS, COMSOL, NI Multisim/LTSpice; oscilloscopes, signal generators, lock-in amplifiers, LCR meters.
- **Programming:** Python (NumPy, pandas, scikit-learn), MATLAB/Simulink, C/C++.

EDUCATION

MEng Electrical & Electronic Engineering — University of Southampton 2021 – 2026

Upper Second-Class Honours (2:1)

Relevant modules: Digital Systems & Microprocessors, Embedded Processors, Advanced Programming, Machine Learning Technologies.

ENGINEERING PROJECTS

Wireless RFID E-Textile Sensor System

Group Project — 85%

- Designed and simulated a dipole antenna with inductive-loop topology in ANSYS HFSS for a wireless e-textile sensor
- Reverse-engineered an undocumented capacitive-sensor topology (a capaciflector) from first principles when the RFID chip's datasheet gave no guidance, then hand-fabricated the flexible PCB
- Validated the complete wireless system from 80 to 160 cm; at the best range, 100 cm, it resolved six clear breathing cycles in the sensor data

NISC Processor Design on FPGA

Individual Coursework — 78%

- Designed and verified a custom SystemVerilog processor on a Cyclone V FPGA (DE1-SoC board), passing all 8 simulation test cases and optimising the architecture to 63 ALMs

Signal Conditioning for an Engine Vibration Accelerometer

Individual Coursework — 70%

- Diagnosed a bridge-impedance mismatch in an initial amplifier design (78% signal loss predicted, 60% in simulation), then fixed it with an instrumentation-amplifier topology that cut the loss to 0.35%

LEADERSHIP & COMMUNICATION

- **President, Malaysian Students' Association (2023)** — led strategy and day-to-day operations; coordinated across teams and stakeholders.
- **Supreme Council, UK & Eire Council (2023)** — debated and shaped organisation-wide policy.

LANGUAGES & REFERENCES

Languages: English (fluent), Malay (native).

References: Available on request.